REMARKS

Claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by Kejriwal *et al.* (U.S. Patent No. 6,704,794; hereinafter "Kejriwal"). Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant adds new claims 6-8 and submits the arguments below in traversal of the claim rejections.

An embodiment of the Applicant's invention relates to a multi-layered packet processing device using multiple processors for processing a received multi-layered packet at a hardware level. The multi-layered packet processing device includes an interface for transmitting a data packet to a node and receiving the data packet from the node through a public network. The embodiment also includes a plurality of packet processing portions for sequentially processing the data packet in a pipeline pattern according to a header of the data packet transferred through the interface.

Kejriwal relates to a cell processing pipeline having a plurality of stages for cell reassembly. The cell has a cell header and a cell payload. One of the stages is configured to parse packet header information located within the cell payload.

Applicant submits that claim 1 is believed to be patentable because each and every element of the claim is not disclosed or suggested by Kejriwal. Claim 1 recites:

> A multi-layered packet processing device, comprising:
>
> an interface of a public network for transmitting a data packet to a node and receiving the data packet from the node through a public network; and

a plurality of packet processing portions for sequentially processing the data packet in a pipeline pattern, according to a header of the data packet transferred from the interface of the public network.

As an example, Kejriwal fails to disclose or suggest a plurality of packet processing portions for sequentially processing the data packet in a pipeline pattern, according to a header of the data packet transferred from the interface of the public network. In the Office Action, the Examiner states that the packet aggregation layer 205, packet processing pipeline 240, and the output packet organizer 250 correspond to the aforementioned feature of claim 1. The packet processing pipeline 240 and the output packet organizer 250, however, do not process the data packet. Instead of receiving the data packet itself, the packet processing pipeline 240 receives control information. Col. 4, lines 18-20. Likewise, the output packet organizer 250 does not process the data packet. Rather, the output packet organizer 250 receives a packet identifier. Col. 3, lines 37-40. Therefore, the packet processing pipeline 240 and the output packet organizer 250 cannot possibly sequentially process the data packet in a pipeline fashion, as claimed.

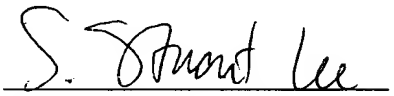
For at least the above reasons, claim 1 is believed to be patentable.

Applicant submits new claims 6-8 to more fully claim the invention. The new claims are believed to be patentable for at least the reasons submitted for the respective base claims.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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*Granted limited recognition under 37 C.F.R. § 11.9(b), as shown in a copy of the same filed on March 14, 2005, at the U.S.P.T.O.

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